Amendments to the Specification

Please amend the specification as indicated.

Please amend the Table of Contents preceding paragraph [0054] as follows:

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Please amend the Heading preceding paragraph [0063] as follows:

Signals corresponding to the eye diagrams as illustrated in FIGS. 1 IA and 11B are difficult to digitize because of the excessive inter-symbol distortion.[[.]]

Please amend the Heading preceding paragraph [0066] as follows:

II. ~~Example Environments~~ Analog Equalization

Please amend the paragraph [0077] as follows:

FIG. 5 is a parallel transceiver 500 implementation of the transceiver 400, wherein multiple transceivers 400A-400D are implemented in parallel. Each analog signal 102A-102D is referred to herein as a channel. Thus, the parallel transceiver 500 is referred to herein as a multi-channel transceiver. In an embodiment, multiple parallel transceivers 500 are implemented on a single integrated circuit ("IC").

Please amend the paragraph [0080] as follows:

U.S. provisional application titled, [[:]]"High-Speed Serial Transceiver," serial number 60/200,813, filed April 28, 2000;

Please amend the paragraph [0081] as follows:

U.S. non-provisional patent application titled, "Phase Interpolator Device and Method," serial number ~~(to be assigned)~~ 09/844,266, attorney docket number 1875.0560005, filed April 30, 2001;

Please amend the paragraph [0082] as follows:

U.S. non-provisional patent application titled, "Timing Recovery and Phase Tracking System and Method," serial number ~~(to be assigned)~~ 09/844,296, attorney docket number 1875.0560002, filed April 30, 2001;

Please amend the paragraph [0083] as follows:

U.S. non-provisional patent application titled, "Timing Recovery and Frequency Tracking System and Method," serial number ~~(to be assigned)~~ 09/844,432, attorney docket number 1875.0560001, filed April 30, 2001; and

Please amend the paragraph [0084] as follows:

U.S. non-provisional patent application titled, "High-Speed Serial Data Transceiver and Related Methods," serial number ~~(to be assigned)~~ 09/844,441, attorney docket number 1875.0560004, filed April 30, 2001;

Please amend the paragraph [0091] as follows:

FIG. 10 is an example router 1000, including a front panel 1002, a ~~back plane~~ backplane 1004 and one or more interfacing circuit boards 1006. Front panel 1002 typically includes a plurality of connectors or "jacks," to which external devices, such as computers, servers, terminals, communications devices, other routers, and the like, can be coupled. The router 1000 receives and transmits (i.e., routes) signals, typically between the external devices. The signals can be electrical and/or optical signals.

Please amend the paragraph [0094] as follows:

Example interfacing circuit board 1006A is now described. Interfacing circuit board 1006A optionally includes one or more interface components 1008 that receive and/or buffer one or more signals received from external devices through the front panel 1002. In the illustrated example, the interface component 1008 receives an optical signal

~~1010~~1001 from the front panel 1002. Accordingly, in this embodiment, interfacing component 1008 includes one or more optical converters that convert the optical signal ~~1010~~1001 to an electrical analog data signal, illustrated here as an analog serial data signal 1012. Additionally, or alternatively, interfacing component 1008 sends and/or receives one or more other analog data signals 1014A-n to/from other external devices through the front panel 1002. Additionally, or alternatively, interfacing component 1008 sends and/or receives one or more of the signals 1014A-n to/from somewhere other than the front panel 1002.

Please amend the paragraph [0098] as follows:

The optional switch fabric 1018 outputs parallel digital data signals 1020 to second transceiver 1022, which can be implemented as one or more of transceivers 400 (FIG. 4), 500 (FIG. 5) and/or 600 (FIG. 6). A transmitter 402 within the transceiver 1022 converts the parallel digital data signals 1020 to serial analog data signals 1024 and transmits them across the ~~back plane~~ backplane1004to one or more other interface circuit boards 1006n, and/or back to interface circuit board 1006A.

Please amend the paragraph [0099] as follows:

One or more receivers 100 within the transceiver 1022 receives analog data signals 1024 from the ~~back plane~~ backplane1004, digitizes them, and converts them to parallel digital data signals 1020. The parallel digital data signals 1020 are provided to the switch fabric 1018, which provides any of a variety of functionalities. The switch

fabric 1018 outputs parallel digital data signals 1016 to one or more transmitters 402 within the transceiver 1010, which converts them to analog data signals for transmission to an external devices, possibly through the interface component 1008 and the front panel 1002.

Please amend the paragraph [0100] as follows:

Additional interface circuit boards 1006n operate in a similar fashion. Alternatively, one or more of the interface circuit boards 1006A-n are configured with more or less than the functionality described above. For example, in an embodiment, one or more of the interface circuit boards 1006A-n are configured to receive analog data signals from the front panel 1002 and to provide them to the ~~back plane~~ backplane1004, but not to receive analog data signals 1024 from the ~~back plane~~ backplane1004. Alternatively, or additionally, one or more of the interface circuit boards 1006A-n are configured to receive analog data signals 1024 from the ~~back plane~~ backplane1004 and provide them to the front panel 1002, but not to receive analog data signals from the front panel 1002.

Please amend the paragraph [0101] as follows:

In an embodiment, equalization parameters adapt in real time. This permits a receiver to adapt to a variety of signal paths. This also permits multiple parallel receivers to independently adapt to their respective associated signal paths. In FIG. 10, for example, in an embodiment, multiple receivers 100 are implemented within transceiver

1022 for receiving analog signals 1024 from the backplane 1004. Typically, each analog signal 1024 arrives at the transceiver 1022 through a different signal path across the backplane 1004 and is thus potentially subject to different inter-symbol distortion. In accordance with the invention, each receiver 100 independently adapts to a respective signal path.

Please amend the paragraph [0112] as follows:

Referring to FIG. 15, the equalizer 106 is illustrated with a sampler 1500 that samples the analog data signal ~~103~~ 102 and outputs discreet-time analog samples ~~1502~~ 1504. In an embodiment, the sampler 1500 includes one or more sample and hold and/or a track and hold circuits. In FIG. 15, the sampler 1500 is illustrated as part of the equalizer ~~1400~~ 106. Alternatively, the sampler 1500 can be outside of the equalizer ~~1400~~ 106.

Please amend the paragraph [0113] as follows:

In operation, the sampler 1500 samples the analog data signal 102 in accordance with the Nyquist theorem and the discreet-time analog FIR ~~1502~~ 1416 operates on discreet-time analog samples 1504 of the analog data signal 102.

Please amend the paragraph [0116] as follows:

In FIG. 19, the discreet-time analog FIR filter 1416 includes a fixed weight 1920 that operates on a present output of the sampler 1500. The discreet-time analog FIR

filter 1416 further includes a tap defined by a delay 1922 and an ~~adjustable~~ variable weight 1924. The ~~adjustable~~ variable weight 1924 operates on a prior output of the sampler 1500. The fixed weight 1920 and the variable weight 1924 scale the present output of the sampler and the prior output of the sampler, respectively, according to values of the respective weights.

Please amend the paragraph [0117] as follows:

The output of the ~~adjustable~~ variable weight 1924 is subtracted from the output of the ~~first~~ fixed weight 1920 in a combiner 1926.

Please amend the paragraph [0121] as follows:

Phase path ~~702~~ 704 preferably takes into account any path delay in the data path 702. One way to take into account delay in data path 702 is to determine the path delay in the data path 702 and design the phase path 704 accordingly.

Please amend the paragraph [0125] as follows:

FIG. 20 is a high level block diagram of an example implementation of the quality measuring and adaptive control module 1402 (FIG. 14[[H]]A, 14F and 14G), including a measuring module 2002 and an equalizer control module 2006. Measuring module 2002 is implemented with analog and/or digital circuitry. Similarly, equalizer control module ~~2004~~ 2006 is implemented with analog and/or digital circuitry.

Please amend the paragraph [0128] as follows:

In a discreet-time analog embodiment, the optional ADC 2004 can be operated at a sub-sample rate with respect to the sampler 1500. In other words, the ADC ~~1904~~ 2004 operates on fewer than every equalized sample from the discreet-time analog FIR filter 1416. For example, in an embodiment, the ADC 2004 operates on every eighth equalized sample from the discreet-time analog FIR filter 1416.

Please amend the paragraph [0130] as follows:

The invention is not, however, limited to these example embodiments. Based on the description herein, one skilled in the relevant art(s) will understand the ADC 2004 can operate on every equalized sample from the FIR filter ~~1502~~ 1416, or any subset and/or off-set thereof.

Please amend the paragraph [0133] as follows:

In an embodiment, the receiver 100 includes the optional quantizer 202, , the quality measuring and adaptive control module 1402 optionally receives the digital data signal 204, and the quality measuring and adaptive control module 1402 compares the equalized analog data signal 104 with the digitized data signal 204. In an example implementation of such an embodiment, the measuring and adaptive control module 1402 utilizes a least-means-squared ("LMS") algorithm to adaptively control the equalizer 106. For example, the LMS algorithm can provide tap updates for the FIR

filter 1412 (FIGs. 14D-H). Any of a variety of conventional LMS methods and/or systems can be utilized.

Please amend the paragraph [0137] as follows:

In an embodiment, the quality measuring and adaptive control module 1402 generates equalizer control signals ~~1410~~ 1404 without utilizing feedback from the quantizer 202.

Please delete the Heading preceding paragraph [00146] as follows:

~~C. Transconductors~~

Please amend the paragraph [0146] as follows:

In an embodiment, the invention utilizes transconductors, or current sources. For example, in an embodiment of the discreet-time analog system FIG. 19, the fixed weight 1920 and the ~~adjustable~~ variable weight 1924 are implemented with transconductors. Furthermore, the discreet-time analog FIR filter 1416 is implemented with differential signals, including "plus" and "minus" differential signals for example. The combiner ~~2008~~ 1926 is then implemented by coupling the plus output from the fixed weight 1920 with the minus output of the variable weight 1924 and by coupling the minus output from the fixed weight 1920 with the plus output of the variable weight 1924.

Please amend the paragraph [0147] as follows:

The example implementations of the discreet-time analog FIR filter 1416 described and illustrated herein are provided for illustrative purposes only. Based on the description herein, one skilled in the relevant art(s) will understand that the discreet-time analog FIR filter 1416 can be implemented in a variety of other ways. For example, and without limitation, additional taps can be utilized, fixed weight 1920 can be replaced with ~~an adjustable~~ a variable weight, and/or variable weight 1924 can be replaced with a fixed weight. Where the discreet-time analog FIR filter 1416 is implemented with fixed weights only, the equalizer 106 is referred to herein as a fixed-weight equalizer.

Please amend the paragraph [0168] as follows:

In an embodiment, step 2602 is ~~are~~ performed at a sub-sample rate relative to the sampling of step 2402.

Please amend the paragraph [0169] as follows:

In an embodiment, step 2602 is ~~are~~ performed at an off-set of a sub-sample rate relative to the sampling of step 2402.

Please amend the paragraph [0182] as follows:

In an embodiment, step 3006 is performed at a sub-sample rate relative to the sampling of step ~~2002~~ 3002.

Please amend the paragraph [0183] as follows:

In an embodiment, step 3006 is performed at an off-set of a sub-sample rate relative to the sampling of step ~~2002~~ 3002.